IN THE CLAIMS

The claims are as follows:

1. (Previously Amended) A semiconductor device with an integrated CMOS circuit with NMOS and PMOS transistors having semiconductor zones which are formed in a silicon substrate and which adjoin a surface thereof, which surface is provided with a layer of gate oxide on which gate electrodes are formed at those areas of the semiconductor zones which form gate zones of these transistors, such that the gate electrodes of the PMOS transistors are formed in a layer of p-type doped polycrystalline silicon and a layer of p-type doped polycrystalline silicon-germanium ($Si_{1-x}Ge_x$; $0<x<1$) situated between said polycrystalline silicon layer and the gate oxide, along with an amorphous silicon layer which is formed, characterized in that the gate electrodes of the NMOS transistors are formed in a layer of n-type doped polycrystalline silicon without germanium.

2. (Original) A semiconductor device as claimed in claim 1, characterized in that the layer of p-type doped polycrystalline silicon-germanium ($Si_{1-x}Ge_x$) contains more than 30 at% of germanium ($x > 0.3$).

3. (Previously Amended) A semiconductor device as claimed in claim 1, characterized in that a less than 5 nm thick layer of amorphous silicon is formed between the gate oxide layer and the layer of polycrystalline silicon-germanium.

4. (Previously Amended) A semiconductor device as claimed in claim 2, characterized in that the semiconductor device comprises besides said PMOS transistors also PMOS transistors having gate electrodes which are formed in a layer of p-type doped polycrystalline silicon without germanium situated on the gate oxide, the latter PMOS transistors being equal to the former in all other respects.

5-8 (Canceled)